Wideband Envelope Elimination and Restoration Power Amplifier with High Efficiency Wideband Envelope Amplifier for WLAN 802.11g Applications

Feipeng Wang, Donald Kimball, Jeremy Popp*, Annie Yang*, Donald Y. C. Lie, Peter Asbeck and Lawrence Larson

Dept. of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA

* Space and Naval Warfare System Center (SPAWAR), San Diego, CA

***Abstract* — This paper presents the design of a silicon bipolar Class-E wideband envelope elimination and restoration (WBEER) power amplifier with a wideband high efficiency envelope amplifier. The envelope amplifier is composed of a linear op-amp stage and a switch buck converter, which achieves high fidelity and high efficiency amplification of wideband high peak to average (PAR) envelope signals. Experimental results show that the envelope amplifier has a bandwidth of 20MHz and 50~60% efficiency. An overall EER power added efficiency (PAE) of 28% at an output power of 19 dBm was achieved for a WLAN OFDM signal at 2.4GHz.**

***Index Terms* — Envelope elimination and restoration, envelope tracking, envelope amplifier, dc-dc converter, hysteretic control, wide bandwidth, power amplifiers, Class E amplifier, Class D amplifier, WLAN, OFDM.**

I. INTRODUCTION

High efficiency power amplifiers (PAs) are critical in portable battery-operated wireless communications because they can dominate the power consumption. The traditional envelope elimination and restoration (EER) system improves the efficiency by driving the radio frequency (RF) transistor in switch mode (Class D/E mode) with a constant amplitude phase signal and superimposing the envelope signal at the collector/drain of RF transistor [1].

This paper presents an improved wideband EER system with an envelope modulated RF phase signal driving a silicon bipolar Class E PA. This approach is especially suitable for wideband high peak–average-ratio (PAR) signals like the OFDM 802.11a/g system (for which the RF bandwidth is 16.56MHz and PAR reaches 8-10dB) [2]. In addition, the use of the Class-E mode and EER configuration allows excellent efficiency and high linearity performance to be achieved in a low-cost silicon-based-technology.

A block diagram of the EER systems is shown in Fig. 1. The highly efficient envelope amplifier is critical to the

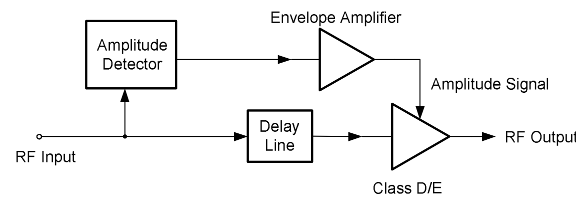

Fig. 1. Block diagram of envelope elimination restoration (EER) system.

EER system since the total system efficiency is the product of the envelope amplifier efficiency and RF transistor drain efficiency, i.e:

$$\eta_{total} = \eta_{envelope\,amp} \cdot \eta_{RF\ transistor} \qquad (1)$$

This paper presents the design considerations for a wideband high efficient envelope amplifier for EER applications in an OFDM system. The wideband envelope amplifier is composed of a parallel linear voltage source and a highly efficient switched current source. This topology has been used for audio amplifier applications, where it improves the fidelity of the class-D switching stage [3]. In this paper, we revisit this topology for wideband envelope amplifier applications. The envelope amplifier analysis, simulation and measurements are compared. The experimental results of EER are shown for application to a WLAN 802.11g system.

II. OFDM ENVELOPE SIGNAL CHARACTERISTICS AND HIGH EFFICIENCY ENVELOPE AMPLIFIER DESIGN

For modern digital modulated signals, the complex baseband signal can be expressed with *I(t)* and *Q(t)* as:

$$s_{BB}(t) = I(t) + jQ(t) \qquad (2)$$

where the envelope signal is:

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$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{3}$$

The nonlinear transformation from *I(t)* and *Q(t)* to the envelope signal *A(t)* will expand the envelope signal bandwidth. Fig. 2 shows the simulated spectrum of the WLAN OFDM baseband and envelope signals. For the OFDM envelope signal, 80% of the energy is concentrated from DC to 250kHz, which implies that a composite amplifier of a wideband high-fidelity voltage source in parallel with a narrowband high-efficient switch source will achieve high overall efficiency.

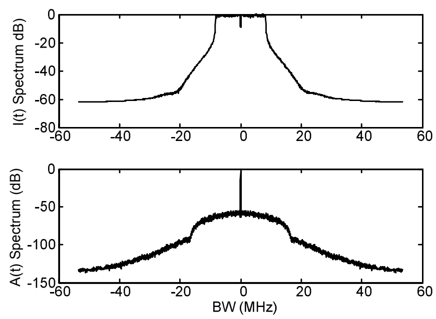

Fig. 2. Spectrum of WLAN 802.11g OFDM baseband *I(t)* and envelope signal *A(t)*.

Fig. 3 shows the concept of the parallel voltage-controlled envelope amplifier. The output voltage is controlled by the voltage source V_C. The current I_{lin} from the voltage source is controlled such that the high efficiency current source I_M provides the majority of the current to the load, as described by :

$$\begin{cases} I_{lin} = I_{load} - I_M \\ I_{load} = \dfrac{V_C}{R_{load}} \end{cases} \quad => I_{lin} \to 0 \;\; as \;\; I_M \to \frac{V_C}{R_{load}} \tag{4}$$

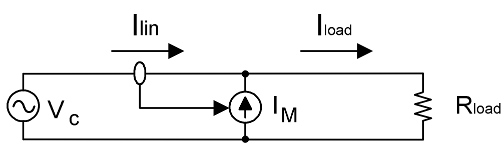

Fig. 3. Topology of the voltage-controlled parallel envelope amplifier.

Fig. 4 shows the circuit implementation of the envelope amplifier using an op-amp as the voltage source (linear stage) and buck converter and inductor as the current source (switch stage). The current source is controlled by a current feedback, with the current flowing out of the linear stage as an error signal and the current to the load as a reference signal. The control scheme is composed of a current sensor resistor R_{sens} and a comparator with hysteresis.

When the input envelope signal is within the power bandwidth of the switch stage, the switch stage provides

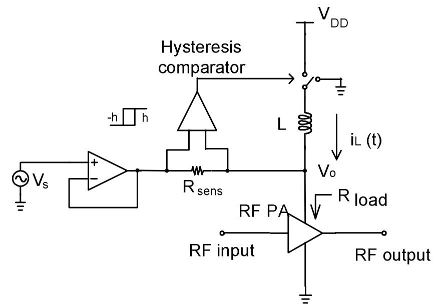

Fig. 4. Circuit implementation of the parallel voltage-controlled envelope amplifier.

the current required by the load, and the linear stage filters out the switch noise. Based on a nonlinear analysis, the average switching frequency for sinewave input signal is calculated to be:

$$f_{sw\_ave} = \frac{R_{sens}}{L} \cdot \frac{V_{DD}}{2h} \left(\frac{V_{s\_dc}}{V_{DD}} - \frac{V^2_{s\_dc}}{V^2_{DD}} - \frac{1}{2} \cdot \frac{V^2_{s\_ac}}{V^2_{DD}} \right) \tag{5}$$

where V_{s_dc} is the dc component of the envelope signal, V_{s_ac} is the fundamental component of the envelope signal, L is the inductance and *h* is the comparator hysteresis voltage. When the input envelope signal is beyond the power bandwidth of the switch stage (either by a large signal at low frequency or a small signal at high frequency), the switch stage enters the voltage saturation region and the current supplied by the linear stage begins to rise to provide power to the load, lowering the overall efficiency.

A plot of the calculated and simulated switching frequency as a function of output level is shown in Fig. 5, and the agreement between the simulation results and (5) is excellent.

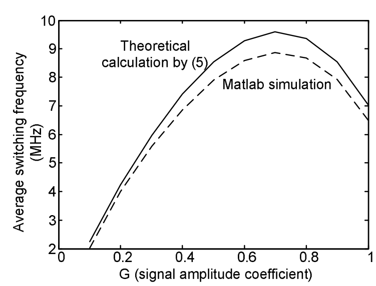

Fig. 5. Theoretical analysis and simulation of average switching frequency for small power bandwidth sinewave signal @ 20kHz. vs. G (signal amplitude coefficient, where $V_{s\_dc} = G \cdot (V_{DD}/2)$, $V_{s\_ac} = 0.9 \cdot G^2 \cdot (V_{DD}/2)$ · V_{DD}=3.3V, h=3.5mV, L=10uH, R_{sens}=1 Ohm, R_{load}=50 Ohm.)

III. MEASUREMENTS OF ENVELOPE AMPLIFIER

The envelope amplifier was measured for different sinewave and OFDM envelope signals. The optimal inductor value of 12 uH was chosen based on trade off between high efficiency and low switching noise for a WLAN 802.11g signal. The switch stage is implemented by using a Fairchild FDV302P PMOSFET. Fig. 6 compares the measured and simulated amplifier behavior for large power bandwidth sinewave signal. Fig. 7 compares the measured and simulated amplifier for the WLAN OFDM signal. The good agreement between simulation and measurement validate the accurate theoretical model of the envelope amplifier. Note that for WLAN OFDM signal, the linear stage provides the high frequency small currents and low frequency peak currents when the switch stage can not follow the slew rate of the input signal. The measured average switching frequency is 5.3MHz, switch stage efficiency is 75%, and the total envelope amplifier efficiency is approximately 50~60% for WLAN 802.11g OFDM signal when the average output power is 140 mW and the peak power is of the order of 1.4 W.

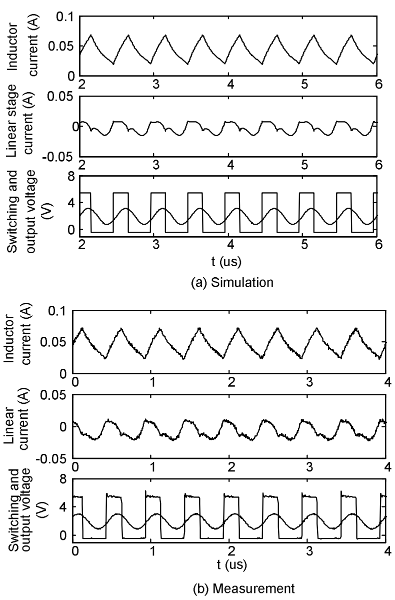

Fig. 6. Simulation and measurement of envelope amplifier for large power bandwidth envelope signal V_{s_dc} = 1.942V, V_{s_ac} = 1.2V. Sinewave frequency is 2MHz. Average switching frequency from both simulation and measurement are 2MHz. The current sensor resistor R_{sens} is 1 Ohm, the load resistor R_{load} is 47 Ohm, the comparator hysteresis value *h* is 7 mV, the power supply is 5.5V and the inductor is 12 uH. In the simulation, 20 ns switching delay is included to model the real circuit switching delay.

IV. EER MEASUREMENTS EXPERIMENTAL RESULTS

A STMicro START499 silicon BJT transistor, ATC RF capacitors, and high Q Coilcraft microCoil inductors were used to implement the Class E RF PA as shown in Fig. 8.

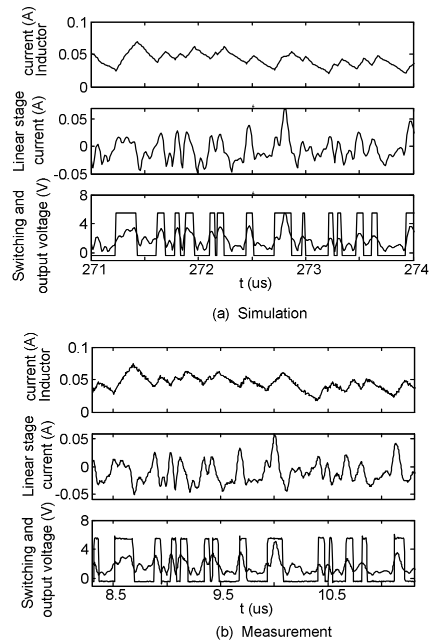

Fig. 7. Simulation and measurement of envelope amplifier for WLAN 802.11g signal. Average switching frequency from simulation is 5.7MHz and from measurement is 5.3 MHz. The simulation and measurement circuit parameters are the same as Fig. 6 measurement.

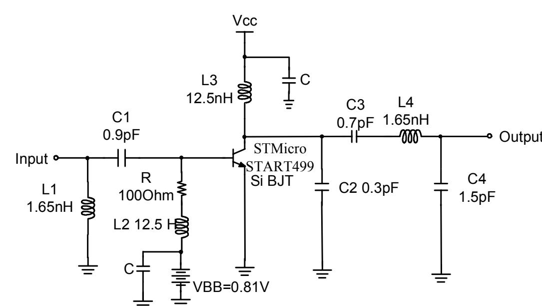

Fig. 8. Class E PA schematic.

Class E analytical design equations [4] and Cadence Spectre simulation with component optimization were done to achieve collector efficiency as high as 75% and a PAE of 57%. It was found that using an "L" impendence matching network on the output designed for 20 ohms and input designed for 35 ohms gave optimum PAE results. Fig. 9 shows Class E PA CW simulation and measurement. Fig. 10 shows the CW performance of Class E PA at different collector voltages at 2.4 GHz. The optimal EER PA efficiency is formed by peak efficiency point of each of the fixed Vcc efficiency curves. The comparison between EER PA and Class AB PA is also shown in Fig. 10.

The EER system for the WLAN 802.11g power amplifier was measured, along with an optimally biased HFET Class-AB power amplifier with fixed $V_{dd,}$ for comparison. Since the EER system has inherent nonlinearity associated with the gain variation, baseband

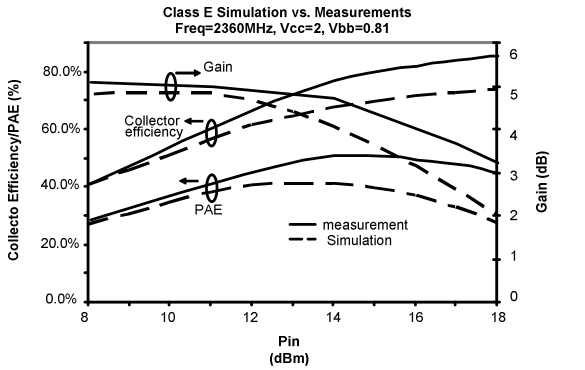

Fig. 9. Simulation and measurement of Class E PA at 2.36GHz when Vcc=2V.

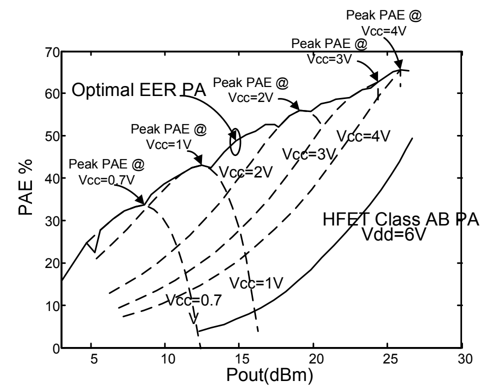

Fig. 10. Measurement of optimal EER PA efficiency obtained by sweeping input power at different collector voltages (under CW condition at 2.4GHz.) The collect voltage V_{cc} is swept from 0V to 4V, but the base voltage V_{bb} is constant at 0.81V. A constant V_{dd} (6V) HFET Class AB PA measurement at 2.4GHz is shown for comparison.

predistortion was implemented to improve the system linearity using a previously published setup [5]. An adaptive time-alignment was also implemented in the EER system and the fine time alignment resolution could be smaller than 0.5ns, satisfying the 802.11g OFDM requirements [6]. Table I shows the comparison of the measured results of the EER amplifier and the constant V_{dd} Class AB RFPA implemented in a GaAs HFET technology for WLAN OFDM signal. The PAE is improved by a factor of more than two.

TABLE I
COMPARISON BETWEEN EER AND CONSTANT V_{dd} HFET CLASS AB RF PA WITH OFDM SIGNAL

	EER Amplifier	Class AB Amplifier
Pout	19 dBm	20 dBm
Gain	6.5 dB	10 dB
Drain/collector efficiency	66 %	13.7 %
RF transistor PAE	51 %	12.3 %
Envelope amplifier efficiency	55 %	-
Overall drain/collector efficiency	36 %	13.7 %
Overall PAE	28 %	12.3 %
EVM	2.8 %	1.6 %

V. CONCLUSION

A wideband high efficiency EER power amplifier employing a high efficiency envelope amplifier has been designed and implemented for application to WLAN 802.11g. The theoretical analysis of the wideband high efficiency envelope amplifier agrees well with the measurement. The efficiency of the envelope amplifier is 50%~60% for WLAN OFDM envelope signals. The EER overall efficiency is 36% at 19 dBm output power, the PAE is greater than 28%, and the linearity requirements are met by implementing the baseband pre-distortion technology and adaptive time-alignment. Compared with a Class AB RFPA, the efficiency and PAE is roughly doubled.

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